Digital Electronics

1) A number expressed in binary 2's complement as 11011.It's decimal equivalent value is
a) 4 b) 5 c) -4 d) -5
= Answer (d) -5
1's complement of 11011
00100
+1
-(00101)
2's complement of 11011
= - (2^4 ×0 + 2^3 ×0 + 2^2 ×1 + 2^1 ×0 + 2^0 ×1)
= - (0 + 0 + 4 + 0 + 1)
= - 5

2) Given $(125)_R$ = $(203)_5$.The value of radix R will be
a) 16 b) 10 c) 8 d) 6
= Answer (d) 6
$(125)_R$ = $(203)_5$
=>1× R^2+2× R^1+5× R^0 = 2× 5^2+0× 5^1+3× 5^0
=>R^2+2R+5 = 50+3
=>R^2+2R-48 = 0
=>R^2+R(8-6)-48 = 0
=>R^2+8R-6R-48 = 0
=>R(R+8)-6(R+8) = 0
=>(R+8)(R-6) = 0
∴R = -8,6
So,R = 6

3) The minimum number of NOR gates required to implement A(A+$\bar{B}$)(A+$\bar{B}$+C) is equal to
a) 0 b) 3 c) 4 d) 7
= Answer (a) 0
A(A+$\bar{B}$)(A+$\bar{B}$+C)
= (A+A$\bar{B}$)(A+$\bar{B}$+C)
= (A+A$\bar{B}$+AC+A$\bar{B}$+A$\bar{B}$+A$\bar{B}$C)
= A+A$\bar{B}$+AC+A$\bar{B}$C
= A(1+$\bar{B}$)+AC(1+$\bar{B}$)
= A+AC [∵ 1+$\bar{B}$ = 1]
= A(1+C)
= A [∵ 1+C = 1]

4) An n bit parallel adder consists of
a) n/2 full adder b) 2n half adder
c) n full adder d) (n+1) full adder
= Answer (c) n full adder

5) Without any additional circuitry,an 8 : 1 MUX can be used o obtain
a) Some but not at all Boolean functions of 3 variables
b) All functions of 3 variables but none of 4 variables
c) All functions of 3 variables and some but not at all of 4 variables
d) All functions of four variables
= Answer (c) All functions of 3 variables and some but not at all of 4 variables

6) A logical expression in the Sum Of Products (SOP) is suitable for implementation using
a) AND gates b) NOR gates c) NAND gates d) EX-OR
= Answer (c) NAND gates

7) In a full adder denoting sum by S and carry by C
a) S = 1 when two or more inputs are unity
b) C = 1 when two or more inputs are unity
c) C = 1 when all the inputs are unity
d) S = 1 when all inputs are unity
= Answer (b) C = 1 when two or more inputs are unity

8) If the number of bits in input and output codes is 4 and 8 respectively for a ROM.The memory of this chip equals to
a) 12 bit b) 32 bit c) 128 bit d) 256 bit
= Answer (c) 128 bit

9) The 'sum' output in a half adder can be realized by using a single two input gate which should be a/a^n
a) Exclusive OR gate b) NOR gate
c) AND gate d) OR gate
= Answer (a) Exclusive OR gate

10) The initial state of MOD-16 down counter is 0110.What will it be after 37 clock pulses?
a) Indeterminate b) 0101 c) 0001 d) 0110
= Answer (c) 0001

11) A certain J-K flip-flop has t_{nd} = 12 ns.The largest MOD ripple counter that can be constructed from these flip-flop and still operate upto 10 MHz is
a) 8 b) 256 c) 512 d) 10
= Answer (b) 256
f = $\frac{1}{nt_d}$
=>10× 10^6 = $\frac{1}{n\times 12\times 10^{-9}}$
=>n = 8
∴ n = 8
2^8 = 256

12) What is frequency of output of the eight flip-flops when the input clock frequency is 512 KHz
a) 16 KHz b) 4 KHz c) 2 KHz d) 8 KHz
= Answer (c) 2 KHz
Output frequency of eight flip-flops

$= \frac{1}{2^8} \times$input frequency
$= \frac{1}{2^8} \times 512$
$= \frac{512}{256}$
$= 2$

13) Which of the following TTL sub-families has maximum speed?
a) Standard TTL b) Schottky-clamped TTL c) High TTL d) Low speed TTL
= Answer (b) Schottky-clamped TTL

14) Which of the following logics possesses highest noise immunity?
a) DTL b) HTL c) ECL d) TTL
= Answer (b) HTL

15) The figure of merit of a logic family is given by
a) gain bandwidth product b) (propagation delay time)×(power dissipation)
c) (noise margin)×(power dissipation) d) (fan-out)×(propagation delay time)
= Answer (b) (propagation delay time)×(power dissipation)

16) In the various logic families are arranged in the descending order of their fan-out capabilities,the sequence will be
a) TTL,ECL,IIL,CMOS B) ECL,TTL,IIL,CMOS
c) IIL,TTL,ECL,CMOS d) CMOS,ECL,TTL,IIL
= Answer (d) CMOS,ECL,TTL,IIL

17) A combinational circuit consists of
a) logic gates only b) memory elements only
c) logic gates and a memory d) None
= Answer (a) logic gates only

18) The operation of gate which commutative but not associative is
a) NOR b) EX-OR c) OR d) AND
= Answer (a) NOR

19) The address bus width of a memory of size 1024×8 bit is
a) 8 bit b) 10 bit c) 13 bit d) 15 bit
= Answer (b) 10 bit

20) The final step in designing the combinational circuit is
a) to determine the input and output variables
b) to draw the truth table
c) to minimize the Boolean function for each output obtained
d) to draw the minimized logic diagram
= Answer (d) to draw the minimized logic diagram

21) Match list (I) with list (II)

List I	**List II**
P. Multiplexer	1. Sequential memory

Q. De-multiplexer
R. Encoder

2. Converts decimal number to binary
3. Data sector
4. Routs out many data output
With single input

Codes

	P	Q	R
a)	4	3	1
b)	2	1	4
c)	1	2	3
d)	3	4	2

	P	Q	R
= Answer (d)	3	4	2

22) Match List I with List II

List I	**List II**
P. TTL	1. Maximum power consumption
Q. ECL	2. Highest packing density
R. n-MOS	3. Least power consumption
S. CMOS	4. Saturated logic

Codes

	P	Q	R	S
a)	4	1	2	3
b)	4	1	3	2
c)	1	4	2	3
d)	1	4	3	2

	P	Q	R	S
= Answer (a)	4	1	2	3

23) A switch tail ring counter is made by using single D flip-flop.The resulting circuit is
a) SR flip-flop b) J-K flip-flop c) T flip-flop d) D flip-flop
= Answer (c) T flip-flop

24) In a sequential circuit,the output at any instant of time depends
a) only on the inputs present at that instant of time
b) on past outputs as well as present inputs
c) only on the past inputs
d) only on the present outputs
= Answer (b) on past outputs as well as present inputs

25) How many flip-flops are required to built a binary counter to count from 0 to 1023?
a) 24 b) 10 c) 6 d) 1
= Answer (b) 10

26) The S and R inputs of S-R flip-flop are called synchronous inputs because
a) when S = 1,$\bar{Q}$ = 0
b) when S = 1,Q = 0
c) the data on these inputs are transferred on the output
d) the data is transferred to output only when clock signal is applied to it

= Answer (d) the data is transferred to output only when clock signal is applied to it

27) For a divide by 4 counter,the present input P is equal to
a) 4 b) 12 c) 8 d) 16
= Answer (b) 12

28) Suppose input to J-K flip-flop is J = 0,K = 1 with applied clock pulse of 20 ms and the propagation delay time of 2 ns.Then the operation performed is
a) flip-flop race around condition
b) flip-flop toggle
c) flip-flop normal operation
d) Both (a) and (b)
= Answer (c) flip-flop normal operation

29) In general block diagram of sequential logic circuit,the clock is given by
a) time delay device b) output logic
c) memory element d) Both (a) and (b)
= Answer (d) Both (a) and (b)

30) To convert a full adder into a full subtractor
a) cannot be converted
b) one input to carry is to be complemented
c) carry is to be complemented
d) sum is to be complemented
= Answer (b) one input to carry is to be complemented

31) In a 4 bit full adder,how many half adders and OR gates are required?
a) 8 and 4 b) 7 and 3 c) 8 and 3 d) 7 and 4
= Answer (b) 7 and 3

32) Full adder circuit can be implemented by
a) multiplexers b) decoders c) half adders d) AND and OR gate
= Answer (a) multiplexers

33) The characteristic equation of the T flip-flop is given by
a) $Q^+ = T\bar{Q} + Q\bar{T}$ b) $Q^+ = TQ + \bar{T}\bar{Q}$ c) $Q^+ = TQ$ d) $Q^+ = T\bar{Q}$
= Answer (a) $Q^+ = T\bar{Q} + Q\bar{T}$

34) D flip-flop is formed by combining the inputs of
a) T flip-flop b) S-R flip-flop c) J-K flip-flop d) Master slave J-K flip-flop
= Answer (b) S-R flip-flop

35) To convert any counter into count down,the gate that can be use is
a) X NOR b) AND c) XOR d) OR
= Answer (c) XOR

36) In standard TTL gates,the totem pole output stage is primarily used to
a) increase the noise margin of the gate

b) decrease the output switching delay
c) facilitate a wired OR logic connection
d) increase the output impedance of the circuit
= Answer (b) decrease the output switching delay

37) The output of a logic gate is 1 when all its inputs are at logic 0.The gate is either
a) a NAND or an EX-OR gate b) a NOR or an EX-OR gate
c) an AND or an EX-NOR gate d) a NOR or an EX-NOR gate
= Answer (d) a NOR or an EX-NOR gate

38) The complete set of only those logic gates designed as universal gate is
a) NOT,OR and AND gates b) XNOR,NOR and NAND gates
c) NOR and NAND gates d) XOR,NOR and NAND gates
= Answer (c) NOR and NAND gates

39) In binary R-2R ladder digital to analog converter,the input resistance for each inputs is
a) 4R b) R c) 2R d) None
= Answer (d) None

40) Th number of comparators in a parallel conversion type 8-bit analog to digital converter is
a) 256 b) 255 c) 16 d) 8
= Answer (b) 255
2^N - 1
=2^8 - 1
= 255

41) The full scale output of a 8-bit digital to analog converter is 0 to 10 V.The percentage resolution is
a) 0.06 V b) 0.04 V c) 0.03 V d) 0.02 V
= Answer (b) 0.04 V
8-bit = 2^8 - 1
= 255 step
Resolution = $\frac{Full\ scale\ output}{Total\ step}$
= $\frac{10}{255}$
= 0.04

42) The resolution of a digital to analog converter is approximately 0.4 % of its full scale range it is
a) a 16-bit converter b) a 12-bit converter
c) a 10-bit converter d) an 8-bit converter
= Answer (d) an 8-bit converter
AS,
$\frac{1}{2^N-1} \leq 0.004$
=>2^N = 251
∴N = 8

43) For a digital input of 1001 the output is 9 mv,Then for digital input of 1100,the analog output will be
a) 9 mv b) 10.5 mv c) 12 mv d) None

= Answer (c) 12 mv
Analog output = K × Digital input
For 1001,digital input = 9
Analog Output = 9
∴K = $\frac{9}{9}$
= 1
For 1100,digital input = 12
∴Analog output = 1 × 12
= 12 mv

44) For digital to analog converter,the maximum full scale output is 16 V,then the resolution after doubling as step size will be
a) half b) same c) double d) four times
= Answer (c) double

45) The resolution of an 8-bit analog to digital converter is
a) 40% b) 0.4% c) 2.0% d) 0.04%
= Answer (b) 0.4%

46) The number of comparisions carried out ina 4-bit flash type analog to digital is
a) 16 b) 15 c) 4 d) 3
= Answer (b) 15
Comparators = 2^N-1
= 2^4-1
= 16-1
= 15

47) A differentiator has transfer function whose
a) phase increases linearly with frequency
b) amplitude remains constant
c) amplitude decreases linearly with frequency
= Answer (b) amplitude remains constant

48) Among the following four,the slowest ADC is
a) parallel comparator (flash) type
b) successive approximation type
c) integrating type
d) counting type
= Answer (c) integrating type

49) The Boolean expression (XYZ+YZ+ZX) after simplification is
a) X b) Y c) Z d) (X+Y)Z
= Answer (d) (X+Y)Z
XYZ+YZ+ZX
= YZ(X+1)+ZX
= YZ+ZX [∵1+X = 1]
= Z(Y+X)

50) An OR gate has 6 inputs.How many input words are there in its truth table?
a) 6 b) 36 c) 64 d) 64000
= Answer (c) 64
Inputs = 6
Words = 2^6
= 64

51) The Boolean function Y = AB + CD is to be realized using only 2-input NAND gates.The minimum number of gates required is
a) 2 b) 3 c) 4 d) 5
= Answer (b) 3

52) The voltage level for negative logic system
a) must necessarily be negative b) must necessarily be positive
c) need not be negative d) mist be necessarily 0 V and 5 V
= Answer (a)) must necessarily be negative

53) The 4-bit 2's complement representation of a decimal number is 1000.The number is
a) +8 b) zero c) -7 d) -8
= Answer (d) -8
-(2's complement of 1000)
= -(1000)
= -($2^3 \times 1$+$2^2 \times 0$+$2^1 \times 0$+$2^0 \times 0$)
= -8

54) Match List I with List II

List I	List II
P. Ripple counter	1. 2^N
Q. Johnson counter	2. N
R. Ring counter	3. 2N
S. Sequence counter	4. 2^N-1

Codes

	P	Q	R	S
a)	1	3	2	4
b)	1	3	2	1
c)	1	2	3	4
d)	4	1	2	3

	P	Q	R	S
= Answer (a)	1	3	2	4

55) A master slave flip-flop has the character that
a) change in the input immediately reflected in the output
b) change in the output occurs when the state of the master is affected
c) change in the output occurs when the state of the slave is affected
d) both the master and the slave states are affected at the same time
= Answer (b) change in the output occurs when the state of the master is affected

56) Express 8^4 in octal system is

a) $(1000)_8$ b) $(10000)_8$ c) $(10100)_8$
= Answer (b) $(10000)_8$

57) A memory system has a total of 8 memory chips,each with 12 address lines and 4 data lines.The total size of the memory system is
a) 6 Kb b) 32 Kb c) 48 Kb d) 64 Kb
= Answer (b) 32 Kb
Each chip 2^{12} = 4096 b
= 4 Kb
Memory size of 8 chip = (8×4) Kb
= 32 Kb